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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,773	09/26/2003	Bunsho Kuramori	030712-13	4336

22204 7590 04/30/2007

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ART UNIT	**PAPER NUMBER**
2816	

MAIL DATE	DELIVERY MODE
04/30/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/670,773
Filing Date: September 26, 2003
Appellant(s): KURAMORI ET AL.

Donald R. Studebacker, Reg. No. 32,815

For Appellant

EXAMINER'S ANSWER

This is in response to the amended appeal brief filed Dec 15, 2006, related to the original appeal brief filed on Aug 29, 2006 appealing the Office action mailed Nov 30, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

However, it is noted that the appellant's brief presents arguments relating to objections of the specification. This issue relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a level shift circuit, does not reasonably provide enablement for a substrate voltage generating circuit. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Although the applicants' own Fig. 1 is identified as a "substrate voltage generating circuit" that apparently generates substrate voltage VBB at its output terminal, wherein VBB is allegedly lower than VSS, the figure and disclosure do not clearly show/disclose how this is actually accomplished. For example, the right terminal of both capacitors c1 and c2 (i.e. corresponding to nodes n1 and n2, respectively), as well as one terminal from each of NMOS transistors SW1 and SW2, are coupled directly to VSS. Therefore, when the gate of the transistors receives a low signal VBB (through inverters INV1 and INV 2, respectively), the transistors will be off and VSS is not coupled to output terminal OUT_vbb. Also at this time, the left terminal of capacitors c1 and c2 will receive high signal VDD (through inverters INV3 and INV 4, respectively), and would charge up towards VDD via the pull-up section of their respective inverter (e.g. INV 3 or INV 4). However when the outputs of inverters INV 1 and INV 2 transition from VBB to VDD, the gate of the corresponding transistor (e.g. SW1 or SW2) receives VDD, and the transistors turn on, coupling VSS to output terminal OUT_vbb. At this time, the left terminal of capacitors c1 and c2 receive VSS (through the pull-down section of their respective inverter INV3 or INV 4), thus discharging the capacitor's previous charge of VDD towards VSS. The applicants admit that transistors/switches SW1 and SW2 are "switched on alternately" (e.g. see the ninth paragraph of VII.A., and the second paragraph of VII.B, within the Appeal Brief). Therefore, it is still not understood how the

claimed invention (e.g. related to the applicants' own Fig. 1) can be a substrate voltage generating circuit that generates/provides a third potential level (e.g. VBB), that is allegedly lower than the second potential level (e.g. VSS), at the output node (e.g. OUT_vbb). The circuit (as shown within Fig. 1), and as claimed in claim 1, would not be able to generate a third potential level (e.g. VBB) lower than the second potential level (e.g. VSS) Therefore, what apparently generates the third potential level, and then applies it to node OUT_vbb, is not shown, disclosed, or claimed. Dependent claims 2-6 carry over the rejection from claim 1.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear in claim 1 how the "output node having a third potential level lower than the second potential level" (line 5), actually relates to the output node being connected to the second power supply node (line 10), which is supplied with the "second potential level" (lines 3-4). For example, when the output node is connected to the second power supply node through the switch circuit, wouldn't the output node have substantially the second potential level instead of the third potential level? Also, since claim 1 is a "substrate voltage generating circuit", how does the voltage at the output node relate to the implied "substrate voltage" the circuit apparently generates? The applicants' use of "an input signal having the first and second potential levels" in claim 1 (line 7), and the use of "the input signal" in claim 2 (lines 3-4 and 5-6) are confusing. It is understood that claim 1 implies the single "input signal" alternates between the first and second potential levels. However, claim 2 cites the same "input signal" is received at the gates of both the first and second transistors, which are connected to the gates of the third and fourth transistors, respectively. As shown in the applicants' own Fig. 2,

and its associated disclosure, the first/second transistors P1/P2 actually receive complementary input signals (i.e. IN and /IN are applied to the gates of P1 and P2, respectively), not the same "input signal" as claim 2 implies. Claim 3 has the same type of problem as claim 2, wherein the first/second transistors do not actually receive the same "input signal" as the limitations on lines 3-6 imply. Both independent claims 7 and 9 also have the same single "input signal" related problem as claims 2 and 3 described above (i.e. the first/second transistors do not both actually receive the same "input signal" as lines 2-5 of each of claims 7 and 9 imply). Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

(10) Response to Argument

The applicant's arguments filed in the amended appeal brief submitted on Dec 15, 2006 have been fully considered, but they are not persuasive.

A. The specification Fully Enables The Subject Matter of Claims 1-6.

The applicants argue that the Examiner has not provided any explanation with respect to various factors and "this rejection cannot stand, as the record does not establish a *prima facie* case of lack of enablement"; and "It is not evident that any experimentation need to be done to carry out the claimed subject matter, let alone undue experimentation. As such, the rejection is improper and should be withdrawn." The descriptions within the Examiner's rejections (e.g. see pages 4-5 of the previous Office Action, and under section 9 described above), and the responses to the arguments (e.g. see section "3" on page 8 of the previous Office Action), have always described the Examiner's interpretation on how the applicants' invention would work with respect to output VBB, the direct connections of VSS to switches SW1,SW2 as shown in the applicants' own Fig. 1, and with respect to the understood alternate on/off operations of switches

SW1,SW2. The applicants' ninth paragraph of the Appeal Brief's section VII.A. cites "VBB at OUT.vbb is generated by making the voltage of capacitor C1 or C2 descend from VSS. Additionally, SW1 and SW2 are switched on alternately. Thus, pulled down voltage VBB is applied to the output node OUT.vbb before the voltage at the output node becoming VSS." However, these generic type statements, along with those in the original disclosure, and also in response to previous Office Actions, have never clearly described how the circuit can actually generate voltage VBB lower than VSS (e.g. VBB is a negative voltage). The applicants also argue "that one of ordinary skill in the art would understand that c1 at node n1 and c2 at node n2, as well as VSS, affect voltage VBB at the output node OUT.vbb." (see the tenth paragraph of section VII.A.), and admit that "switches SW1 and SW2 are switched on alternately" (e.g. see the ninth and second paragraphs under sections VII.A. and VII.B., respectively; it is understood that SW1 will be conducting when SW2 is off, and vice versa). However, with this type of alternate switching, one of ordinary skill in the art would actually understand that node OUT.vbb will be continuously connected to VSS through the switch that is conducting at the time. Although the applicants cite "the node n1 goes "L", i.e. the substrate voltage VBB level by the capacitance element C1...When the switch element SW1 turns ON, the substrate voltage VBB is transferred to the output node OUT.vbb" on page 13, lines 13-17 of the original disclosure, this operation will not occur as cited as long as nodes n1 and n2 are directly coupled to VSS as shown in the applicants' Fig. 1. VBB would not be generated by the circuitry as shown in the applicants' own Fig. 1 since SW1, and/or SW2, will transfer voltage VSS to node OUT.vbb. Therefore, third potential VBB at node OUT.vdd would be equivalent to second potential VSS, and not lower than VSS. [Note: Level shifters 101 and 102 receive VBB, and provide it as the

low level output of the level shifter. Therefore, these level shifters also do not actually generate VBB.] Until the applicants can clearly describe in detail how the output node of the present invention can have a third potential level (e.g. VBB) lower than the second potential level (e.g. VSS) as cited within independent claim 1, the rejections of claims 1-6 described in the previous Office Action, and within this Examiner's Answer, will be maintained. The applicants also cite "if a claim adequately defines patentable subject matter and meets the disclosure and clarity standards of Section 112, then it is proper, even though it may encompass less than what the invention could claim", and "the teaching in the specification must not be ignored" within the thirteenth paragraph of section VII.A. of the Appeal Brief. However, even after re-reading and re-considering the teachings in the original specification, and the various arguments/comments within the previous responses, including the Appeal Brief, it is still not known how the applicants' present invention can generate a third potential level lower than the second potential. Therefore, the claims and disclosures do not adequately define, nor do they meet the disclosure and clarity standards, as previously described above, and the claim rejections are deemed proper.

B. Claims 1-10 Recite Definite Subject Matter

Similar to the rejections/arguments described above, the applicants cite "as SW1 and SW2 switch on alternatively and cooperate via feedback with the rest of the level shifting circuit to produce VBB and not VSS" in the second paragraph of the Appeal Brief's section VII.B. However, as understood by one of ordinary skill in the art from the circuit shown in the applicants' own Fig. 1, when either switch SW1 or SW2 is switched on, VSS will be transferred to output node OUT.vbb, making VBB equivalent to VSS as previously described. This is because nodes n1 and n2 are directly connected to VSS, and will be maintained at the VSS level,

even though their corresponding capacitor (i.e. c1 and c2) will be alternately charged and discharged at the capacitor node coupled to the output of the corresponding inverter (i.e. INV 3 and INV 4). With respect to the use of "input signal" within each of claims 2, 3, 7, and 9, the applicants admit in the third paragraph of section VII.B. that "the input signal to the first transistor P1 is complementary to the input signal transistor P2 as shown in Fig. 2", and that "there is no confusion between "an input signal having the first and second potential levels" in claim 1 and the use of "the input signal" in claim 2." However, a signal with first and second potential levels is not the same signal as its complement (inverse), which also has first and second potential levels. For example, when one signal has the first potential level, the complementary (inverse) signal has the second potential level. As presently cited within each of claims 2, 3, 7, and 9, both the first and second transistors receive the same "input signal." Since the transistors receiving that "input signal" have the same (i.e. first) conductivity type, the transistors will both be either on or off at the same time. The fourth paragraph of section VII.B. indicates the signal has first/second potential levels, and the first/second transistors receive an input signal in a complementary nature. As shown in Figs. 2 and 3, the first/second transistors (i.e. P1/P2 of Fig. 2; P31/P32 of Fig. 3) do receive complementary signals IN and /IN, but these signals are not the same "input signal." Therefore the first/second transistors "receiving the input signal" at their gates, as cited within each of claims 2, 3, 7, and 9 are confusing. The applicants also cite that "claims are not to be read in a vacuum, but rather in light of Appellant's disclosure and interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made" in the seventh paragraph of section VII.B. Although this is true, one must not read limitations from the disclosure into the claims. In this

case, the recited "the input signal" clearly implies a single, distinct signal, wherein none of the recited limitations identify first/second signals, a signal and its complement, or any other type of signals that are distinct from one another. This makes these claims confusing. The dependent claims carry over the rejection(s) from any claim(s) upon which they depend.

C. The Specification Does Not Contain Informalities

The appellants' brief presents arguments relating to the objections to the disclosure. These issues relate to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Terry L. Englund

Conferees:

David Blum

Rexford Barnie R.B 04/25/07

Terry L. Englund